REMARKS

Claims 1 through 7, 9 through 16 and 18 through 20 are currently pending in the application. Please amend claim 1, 13 and 20 as amended herein.

This amendment is in response to the final Office Action of November 5, 2003.

35 U.S.C. § 103(a) Obviousness Rejections

Obviousness Rejection Based on Dea (U.S. Patent No. 5,469,208) in view of So (U.S. Patent No. 5,909,559)

Claims 1 through 5, 7, 10, 12 and 20 are rejected under 35 U.S.C. § 103(a) as being unpatentable over Dea (U.S. Patent No. 5,469,208) in view of So (U.S. Patent No. 5,909,559). Applicant respectfully traverses this rejection, as hereinafter set forth.

M.P.E.P. 706.02(j) sets forth the standard for a Section 103(a) rejection:

> To establish a *prima facie* case of obviousness, three basic criteria must be met. First, there must be some suggestion or motivation, either in the references themselves or in the knowledge generally available to one of ordinary skill in the art, to modify the reference or combine reference teachings. Second, there must be a reasonable expectation of success. Finally, **the prior art reference (or references when combined) must teach or suggest all the claim limitations.** The teaching or suggestion to make the claimed combination and the reasonable expectation of success must both be found in the prior art, and not based on applicant's disclosure. *In re Vaeck*, 947 F.2d 488, 20 USPQ2d 1438 (Fed. Cir. 1991). (Emphasis added).

The 35 U.S.C. § 103(a) obviousness rejections of claims 1-5, 7, 10, 12 and 20 are improper because the elements for a *prima facie* case of obviousness are not met. Specifically, the rejection fails to meet the criterion that the prior art references must teach or suggest all the claim limitations.

The current Office Action states:

> applicant argues that . . . Applicant's apparatus for assisting in compressing video includes at least two separate interfaces, namely a video input port for coupling with the streaming video data from a video unit and a memory interface of the result buffer. Separate interfaces are not disclosed by Dea and So.

In response, the examiner respectfully disagrees. First of all, it is noted that **the alleged "two separate interfaces' is not recited in the claims**. (Office Action, p. 2; emphasis added).

Applicant has amended the independent claims to more clearly and explicitly recite the limitations of the two separate interfaces, which separate interfaces are not taught or suggested by Dea or So or any combination thereof.

Claim 1

Applicant previously, in claim 1, claimed "a result buffer . . . configured to couple with the system memory" and now Applicant claims "a result buffer . . . further including a memory interface configured to couple with the system memory via a first bus independent of a second bus for coupling the central processing unit". Clearly, Applicant, at least in the presently amended claim 1, explicitly claims two separate interfaces which are not taught or suggested by Dea and So or any combination thereof.

Regarding amended independent claim 1, Applicants claim:

> 1. An apparatus for assisting in compressing video data in a computer system including a central processing unit and a system memory, comprising:
> a **video input port configured to electrically couple to a video unit** for receiving video data for a current video frame **from streaming video data**;
> a video input buffer coupled to the video input port for storing the video data from the video input port;
> a previous frame buffer for storing at least a portion of a previous video frame;
> an operation unit coupled to the video input buffer and the previous frame buffer for computing a difference frame from data from the video input buffer and data from the previous frame buffer; and
> a **result buffer coupled to the operation unit, the result buffer further including a memory interface configured to couple with the system memory via a first bus independent of a second bus configured for coupling with the central processing unit**, the result buffer for temporarily buffering the difference frame prior to storing the difference frame in the system memory, the apparatus configured to operate within a north bridge chip of the computer system to enable the central processing unit to retrieve the difference frame directly from the system memory via the north bridge chip for further compression of the video data by the central processing unit. (Emphasis added.)

Regarding claim 1, Dea and So do not appear to teach or suggest an apparatus for assisting in compressing video data in a computer system including a central processing unit and a system memory, comprising: "**a video input port** configured to electrically couple to a video unit for receiving video data for a current video frame from streaming video data; a video input buffer coupled to the video input port . . .; a previous frame buffer . . .; an operation unit coupled to the video input buffer and the previous frame buffer . . .; and a result buffer coupled to the operation unit, the result buffer further including a **memory interface** configured to couple with a system memory via a first bus independent of a second bus configured for coupling with the central processing unit . . ." as claimed by Applicants. Specifically, Applicants' apparatus for assisting in compressing video includes at least **two separate** interfaces, namely a video input port for coupling with the streaming video data from a video unit and a memory interface of the result buffer. Separate interfaces are not disclosed by Dea or So.

Specifically, Dea teaches or suggests, and the previous Office Action concurs, that the Dea architecture is bus oriented with the "apparatus" 120 of Dea being memory mapped to the bus with the bus being the only input and output from the "apparatus." Specifically, Dea teaches or suggests that "[t]he information regarding the current frame line is received from bus interface 200", (col. 6, lines 41-43) and "[w]hen accelerator 120 initiates actions it fetches thirty-two bit words from memory [and] [w]hen accelerator 120 is a target it responds to all scalar accesses or addresses in its range", (col. 5, lines 2-5). Furthermore, according to Dea, "[t]ransmission . . . from . . . store buffer 248 to devices external to accelerator 120 is by way of accelerator bus interface 200." (Col. 7, lines 42-44.) Such a bus architecture is further visibly supported by FIG. 2 of Dea.

The current Office Action dismissed Applicant's argument by stating:

> Dea teaches the accelerator 120 within remote video interface system that has a straight pipeline architecture rather than shared resource which as taught at column 5, lines 25-27. However, it does not restrict the accelerator 120 or the processor 112 to utilize the DRAM 114 (system memory) of the system that is external to the processor 112 or accelerator 120. In support, the passage from column 9, line 65-column 10, line 11 and Fig. 2, whereas the passage describes that the accelerator 120 (core logic unit) includes blocks 238, 246 that perform further encoding operation and stores the encoded data in buffer 248. Furthermore, passage from column 11, lines 5-13, which additionally teaches that "the data as run/value pair for run length encoder 246 are applied by way of line 330

> to encode output circular buffer 332. The data within encode output circular buffer 332 is then applied to variable length encoder 112b". Therefore the above excerpt has clearly demonstrated that the storing of the different frame (encoded data frame) in the system memory (memory 114). (Office Action, p. 3).

The Office Action's citations of Dea, are all supported by the architecture as illustrated in FIG. 2 of Dea. While Dea may utilize the terminology of "straight pipeline architecture rather than shared resources" (see col. 5, lines 27-28), the accelerator 120 of Dea only teaches or suggests and is only illustrated as a device that has **only a single interface**, namely bus interface 200 which attaches to **both** the current frame memory 204 and the encoded store buffer 248 (see the dashed line on the right of FIG. 2 connecting both to a single bus interface 200).

Regarding the So reference, the Office Action cites So because it "discloses that a VSP (wrapper-and-digital signal processor-core) used as a graphic accelerator is provide either as the North bridge or AGP graphic/video chip as described at column 17, lines 24-43." (See Office Action p. 5). Generally, So incorporates digital signal processors (DSPs) at one or more of the bridges, such as at the North bridge and/or South bridge so that the compression and decompression may occur inside of the DSPs of the bridges. So engages in additional compression/decompression complexity within the North bridge and does not teach or suggest an apparatus for assisting in compressing video data in a computer system including a central processing unit and a system memory, comprising: "a **video input port** configured to electrically couple to a video unit for receiving video data for a current video frame from streaming video data; a video input buffer coupled to the video input port . . .; a previous frame buffer . . .; an operation unit coupled to the video input buffer and the previous frame buffer . . .; and a result buffer coupled to the operation unit, the result buffer further including a **memory interface** configured to couple with a system memory via a first bus independent of a second bus configured for coupling with the central processing unit . . ." as presently claimed by Applicants. Therefore, Applicants respectfully request that the rejection to claim 1 be withdrawn.

Claims 2-5, 7, 10 and 12

Regarding claims 2-5, 7, 10 and 12, each of these claims includes additional elements that further distinguish from the cited references. In addition to claims 2-5, 7, 10 and 12 depending either directly or indirectly from amended independent claim 1, each of these claims, as a whole, distinguish over the cited references. Therefore, Applicants respectfully request that the rejections to claims 2-5, 7, 10 and 12 be withdrawn.

Claim 20

Applicant previously, in claim 20, claimed "a result buffer . . . configured to couple with the system memory" and now Applicant claims "a result buffer . . . further including a memory interface configured to couple with the system memory via a first bus independent of a second bus for coupling the central processing unit". Clearly, Applicant, at least in the presently amended claim 20, explicitly claims two separate interfaces which are not taught or suggested by Dea or So or any combination thereof.

Regarding amended independent claim 20, Applicants claim:

> 20. A computer system including resources for compressing video, comprising:
> a central processing unit and system memory for further compressing the video within the computer system;
> a **video input port configured to electrically couple to a video unit** for receiving video data for a current video frame **from streaming video data**;
> a video input buffer coupled to the video input port for storing the video data from the video input port;
> a previous frame buffer for storing a least a portion of a previous video frame;
> an operation unit coupled to the video input buffer and the previous frame buffer for computing a difference frame from data from the video input buffer and data from the previous frame buffer; and
> a **result buffer coupled to the operation unit, the result buffer further including a memory interface configured to couple with the system memory via a first bus independent of a second bus configured for coupling with the central processing unit**, the result buffer for temporarily buffering the difference frame prior to storing the difference frame in the system memory, the video input port, the video input buffer, the previous frame buffer, the operation unit, and the result

> buffer configured to operate within a north bridge chip of the computer system to enable the central processing unit to retrieve the difference frame directly from the system memory via the north bridge chip for further compression of the video data by the central processing unit. (Emphasis added.)

Regarding claim 20, Dea and So do not appear to teach or suggest a computer system including resources for compressing video, comprising: "a central processing unit and system memory . . .; a **video input port** configured to electrically couple to a video unit for receiving video data for a current video frame from streaming video data; a video input buffer coupled to the video input port . . .; a previous frame buffer . . .; an operation unit coupled to the video input buffer and the previous frame buffer . . .; and a result buffer coupled to the operation unit, the result buffer further including a **memory interface** configured to couple with a system memory via a first bus independent of a second bus configured for coupling with the central processing unit . . ." as claimed by Applicants. Specifically, Applicants' computer system including resources for compressing video includes at least **two separate** interfaces, namely a video input port for coupling with the streaming video data from a video unit and a memory interface of the result buffer. Separate interfaces are not taught or suggested by Dea or So or any combination thereof.

As previously stated, Dea's architecture is bus oriented with the resources for compressing video being memory mapped to the bus with the bus being the only input and output path. Applicants reiterate the above-arguments, namely, Dea teaches or suggests that "[t]he information regarding the current frame line is received from bus interface 200", (col. 6, lines 41-43) and "[w]hen accelerator 120 initiates actions it fetches thirty-two bit words from memory [and] [w]hen accelerator 120 is a target it responds to all scalar accesses or addresses in its range", (col. 5, lines 2-5). Furthermore, according to Dea, "[t]ransmission . . . from . . . store buffer 248 to devices external to accelerator 120 is by way of accelerator bus interface 200." (Col. 7, lines 42-44.) Such a bus architecture is further visibly supported by FIG. 2 of Dea.

Regarding the So reference, Applicants sustain the previous arguments regarding the lack of teaching or suggestion of Applicants' claim elements with regard to claim 20. Therefore, Applicants respectfully request that the rejection to claim 20, be withdrawn.

Obviousness Rejection Based on Dea and So and further in view of Abramatic et al. (U.S. Patent No. 4,546,383)

Claims 6 and 13 through 16 are rejected under 35 U.S.C. § 103(a) as being unpatentable over Dea and So and further in view of Abramatic et al. (U.S. Patent No. 4,546,383). Applicant respectfully traverses this rejection, as hereinafter set forth.

M.P.E.P. 706.02(j) sets forth the standard for a Section 103(a) rejection:

> To establish a *prima facie* case of obviousness, three basic criteria must be met. First, there must be some suggestion or motivation, either in the references themselves or in the knowledge generally available to one of ordinary skill in the art, to modify the reference or combine reference teachings. Second, there must be a reasonable expectation of success. Finally, **the prior art reference (or references when combined) must teach or suggest all the claim limitations.** The teaching or suggestion to make the claimed combination and the reasonable expectation of success must both be found in the prior art, and not based on applicant's disclosure. *In re Vaeck*, 947 F.2d 488, 20 USPQ2d 1438 (Fed. Cir. 1991). (Emphasis added).

The 35 U.S.C. § 103(a) obviousness rejections of claims 6 and 13-16 are improper because the elements for a *prima facie* case of obviousness are not met. Specifically, the rejection fails to meet the criterion that the prior art references must teach or suggest all the claim limitations.

Claim 6

Regarding claim 6, Dea, So, and Abramatic, either individually, or in any proper combination, do not teach, suggest, or motivate Applicants' invention of claim 6. Applicants sustain the arguments above that nothing within the four-corners of the cited references teach each and every element of Applicants' invention as claimed, including the elements of the base claim from which claim 6 depends. Namely, Dea, So, and Abramatic do not teach or suggest an apparatus for assisting in compressing video data in a computer system including a central processing unit and a system memory, comprising: "a **video input port** configured to electrically couple to a video unit for receiving video data for a current video frame from streaming video data; a video input buffer coupled to the video input port . . .; a previous frame buffer . . .; an operation unit coupled to the video input buffer and the previous frame buffer . . .; and a result

buffer coupled to the operation unit, the result buffer further including a **memory interface** configured to couple with a system memory via a first bus independent of a second bus configured for coupling with the central processing unit . . ." as claimed by Applicants' claim 6. Therefore, Applicants respectfully request that the rejection to claim 6 be withdrawn.

Claims 13-16

Regarding claims 13-16, Dea, So, and Abramatic, either individually, or in any proper combination, do not teach, suggest, or motivate Applicants' invention of claims 13-16.

Regarding amended independent claim 13, Applicants claim:

> 13. An apparatus for compressing video data in a computer system including a central processing unit, comprising:
>
> a **video input port configured to electrically couple to a video unit** for receiving video data for a current video frame **from streaming video data**;
>
> a video input buffer coupled to the video input port for storing the video data from the video input port;
>
> a previous frame buffer for storing a least a portion of a previous video frame;
>
> an exclusive-OR unit coupled to the video input buffer and the previous frame buffer for computing a difference frame from data from the video input buffer and data from the previous frame buffer;
>
> a result buffer coupled to the exclusive-OR unit for temporarily buffering the difference frame;
>
> a **memory port** coupled to the previous frame buffer and the result buffer, the memory port **independent from the video input port**; and
>
> a **system memory coupled to the memory port** for storing the video data from the video input port and the difference frame from the result buffer, wherein the video data is stored to in a current frame in the memory, the apparatus configured to operate within a north bridge chip of the computer system to enable the central processing unit to retrieve the difference frame directly from the system memory via the north bridge chip for further compression of the video data by the central processing unit. (Emphasis added.)

Regarding claim 13, Dea, So and Abramatic do not appear to teach or suggest an apparatus for assisting in compressing video data in a computer system including a central

processing unit, comprising: "a **video input port** configured to electrically couple to a video unit for receiving video data for a current video frame from streaming video data; a video input buffer coupled to the video input port . . .; a previous frame buffer . . .; an exclusive-OR unit coupled to the video input buffer and the previous frame buffer . . .; and a result buffer coupled to the exclusive-OR unit . . .; a **memory port** coupled to the previous frame buffer and the result buffer, the memory port **independent from the video input port**; and a system memory coupled to the memory port . . ." as claimed by Applicants. Specifically, Applicants' apparatus for assisting in compressing video includes at least a separate video input port for coupling with the streaming video data from a video unit and a memory port for coupling with the system memory. Separate interfaces are not taught or suggested by Dea, So or Abramatic or any combination thereof.

As previously stated, Dea discloses and the Office Action concurs that the Dea architecture is bus-oriented with the "apparatus" 120 of Dea being memory mapped to the bus with the bus being the only input and output from the "apparatus." Specifically, Dea teaches or suggests that "[t]he information regarding the current frame line is received from bus interface 200", (col. 6, lines 41-43) and "[w]hen accelerator 120 initiates actions it fetches thirty-two bit words from memory [and] [w]hen accelerator 120 is a target it responds to all scalar accesses or addresses in its range", (col. 5, lines 2-5). Furthermore, according to Dea, "[t]ransmission . . . from . . . store buffer 248 to devices external to accelerator 120 is by way of accelerator bus interface 200." (Col. 7, lines 42-44.) Such a bus architecture is further visibly supported by FIG. 2 of Dea.

The Office Action cites Dea and So for their alleged teaching or suggestion as previously herein rebutted. The Office Action continues by citing Abramatic for teaching "that XOR function for the difference calculation 56 which has the advantage of providing a less complicated means for the difference calculation techniques as elucidated at column 7, lines 32-35." (See Office Action p. 14).

Applicants sustain the arguments above that nothing within the cited references teach or suggest each and every element of Applicants' invention as claimed in amended independent claim 13. Specifically, Dea, So, and Abramatic do not teach, suggest, or motivate an apparatus

for compressing video data in a computer system including a central processing unit, comprising: "a video input port configured to electrically couple to a video unit for receiving video data for a current video frame from streaming video data; a video input buffer coupled to the video input port . . .; a previous frame buffer . . .; an exclusive-OR unit coupled to the video input buffer and the previous frame buffer . . .; and a result buffer coupled to the exclusive-OR unit . . .; a memory port coupled to the previous frame buffer and the result buffer, the memory port independent from the video input port; and a system memory coupled to the memory port . . ." as claimed by Applicants' amended independent claim 13. Therefore, Applicants respectfully request that the rejection to amended independent claim 13 be withdrawn.

Claims 14-16, 18 and 19

Regarding claims 14-16, 18 and 19, each of these claims includes additional elements that further distinguish from the cited references. In addition to claims 14-16, 18 and 19 depending either directly or indirectly from amended independent claim 13, each of these claims, as a whole, distinguish over the cited references. Therefore, Applicants respectfully request that the rejections to claims 14-16, 18 and 19 be withdrawn.

Obviousness Rejection Based on Dea and So in view of Yan (U.S. Patent No. 5,438,374)

Claim 9 is rejected under 35 U.S.C. § 103(a) as being unpatentable over Dea and So in view of Yan (U.S. Patent No. 5,438,374). Applicant respectfully traverses this rejection, as hereinafter set forth.

M.P.E.P. 706.02(j) sets forth the standard for a Section 103(a) rejection:

> To establish a *prima facie* case of obviousness, three basic criteria must be met. First, there must be some suggestion or motivation, either in the references themselves or in the knowledge generally available to one of ordinary skill in the art, to modify the reference or combine reference teachings. Second, there must be a reasonable expectation of success. Finally, **the prior art reference (or references when combined) must teach or suggest all the claim limitations.** The teaching or suggestion to make the claimed combination and the reasonable expectation of success must both be found in the prior art, and not based on applicant's disclosure. *In re Vaeck*, 947 F.2d 488, 20 USPQ2d 1438 (Fed. Cir. 1991). (Emphasis added).

The 35 U.S.C. § 103(a) obviousness rejection of claim 9 is improper because the elements for a *prima facie* case of obviousness are not met. Specifically, the rejection fails to meet the criterion that the prior art references must teach or suggest all the claim limitations.

Regarding claim 9, Dea, So, and Yan, do not teach or suggest an apparatus for assisting in compressing video data in a computer system including a central processing unit and a system memory, comprising: "a **video input port** configured to electrically couple to a video unit for receiving video data for a current video frame from streaming video data; a video input buffer coupled to the video input port . . .; a previous frame buffer . . .; an operation unit coupled to the video input buffer and the previous frame buffer . . .; and a result buffer coupled to the operation unit, the result buffer further including a **memory interface** configured to couple with a system memory via a first bus independent of a second bus configured for coupling with the central processing unit . . ." as claimed by Applicants' claim 9. Therefore, Applicants respectfully request that the rejection to claim 9 be withdrawn.

Obviousness Rejection Based on Dea and So in view of Hardiman (U.S. Patent No. 5,926,223)

Claim 11 is rejected under 35 U.S.C. § 103(a) as being unpatentable over Dea and So in view of Hardiman (U.S. Patent No. 5,926,223). Applicant respectfully traverses this rejection, as hereinafter set forth.

M.P.E.P. 706.02(j) sets forth the standard for a Section 103(a) rejection:

> To establish a *prima facie* case of obviousness, three basic criteria must be met. First, there must be some suggestion or motivation, either in the references themselves or in the knowledge generally available to one of ordinary skill in the art, to modify the reference or combine reference teachings. Second, there must be a reasonable expectation of success. Finally, **the prior art reference (or references when combined) must teach or suggest all the claim limitations.** The teaching or suggestion to make the claimed combination and the reasonable expectation of success must both be found in the prior art, and not based on applicant's disclosure. *In re Vaeck*, 947 F.2d 488, 20 USPQ2d 1438 (Fed. Cir. 1991). (Emphasis added).

The 35 U.S.C. § 103(a) obviousness rejection of claim 11 is improper because the elements for a *prima facie* case of obviousness are not met. Specifically, the rejection fails to meet the criterion that the prior art references must teach or suggest all the claim limitations.

Regarding claim 11, Dea, So, and Hardiman, either individually, or in any proper combination, do not teach, suggest, or motive Applicants' invention as claimed in claim 11, including all of the claim limitations of the base claim, namely, do not teach or suggest an apparatus for assisting in compressing video data in a computer system including a central processing unit and a system memory, comprising: "a **video input port** configured to electrically couple to a video unit for receiving video data for a current video frame from streaming video data; a video input buffer coupled to the video input port . . .; a previous frame buffer . . .; an operation unit coupled to the video input buffer and the previous frame buffer . . .; and a result buffer coupled to the operation unit, the result buffer further including a **memory interface** configured to couple with a system memory via a first bus independent of a second bus configured for coupling with the central processing unit . . ." as claimed by Applicants' claim 11. Therefore, Applicants respectfully request that the rejection to claim 11 be withdrawn.

Obviousness Rejection Based on Dea, So and Abramatic et al. as applied to claim 13 above, and further in view of Yan

Claim 18 rejected under 35 U.S.C. § 103(a) as being unpatentable over the system of Dea, So and Abramatic et al. as applied to claim 13 above, and further in view of Yan. Applicant respectfully traverses this rejection, as hereinafter set forth.

M.P.E.P. 706.02(j) sets forth the standard for a Section 103(a) rejection:

> To establish a *prima facie* case of obviousness, three basic criteria must be met. First, there must be some suggestion or motivation, either in the references themselves or in the knowledge generally available to one of ordinary skill in the art, to modify the reference or combine reference teachings. Second, there must be a reasonable expectation of success. Finally, **the prior art reference (or references when combined) must teach or suggest all the claim limitations.** The teaching or suggestion to make the claimed combination and the reasonable expectation of success must both be found in the prior art, and not based on applicant's disclosure. *In re Vaeck*, 947 F.2d 488, 20 USPQ2d 1438 (Fed. Cir. 1991). (Emphasis added).

The 35 U.S.C. § 103(a) obviousness rejection of claim 18 is improper because the elements for a *prima facie* case of obviousness are not met. Specifically, the rejection fails to meet the criterion that the prior art references must teach or suggest all the claim limitations.

Regarding claim 18, Dea, So, Abramatic, and Yan, either individually, or in any proper combination, do not teach, suggest, or motive Applicants' invention as claimed, namely, Dea, So, Abramatic and Yen do not appear to teach or suggest an apparatus for assisting in compressing video data in a computer system including a central processing unit, comprising: "a video input port configured to electrically couple to a video unit for receiving video data for a current video frame from streaming video data; a video input buffer coupled to the video input port . . .; a previous frame buffer . . .; an exclusive-OR unit coupled to the video input buffer and the previous frame buffer . . .; and a result buffer coupled to the exclusive-OR unit . . .; a memory port coupled to the previous frame buffer and the result buffer, the memory port independent from the video input port; and a system memory coupled to the memory port . . ." as claimed by Applicants. Specifically, Applicants' apparatus for assisting in compressing video includes at least a separate video input port for coupling with the streaming video data from a video unit and a memory port for coupling with the system memory. In support, Applicants sustain the arguments above as applied to the base claim. Therefore, since Dea, So, Abramatic or Yan, either individually or in any proper combination, do not teach, suggest, or motivate Applicants' invention as claimed in claim 18, Applicants respectfully request that the rejection to claim 18 be withdrawn.

Obviousness Rejection Based on U.S. Patent No. 5,469,208 to Dea in View of U.S. Patent No. 5,909,559 to So, in View of U.S. Patent No. 4,546,383 to Abramatic and further in view of U.S. Patent No. 5,926,223 to Hardiman.

Claim 19 stands rejected under 35 U.S.C. § 103(a) as being unpatentable over Dea (U.S. Patent No. 5,469,208) in view of So (U.S. Patent No. 5,909,559) in view of Abramatic (U.S. Patent No. 4,546,383) and further in view of Hardiman (U.S. Patent No. 5, 926, 223). Applicants respectfully traverse this rejection, as hereinafter set forth.

M.P.E.P. 706.02(j) sets forth the standard for a Section 103(a) rejection:

> To establish a *prima facie* case of obviousness, three basic criteria must be met. First, there must be some suggestion or motivation, either in the references themselves or in the knowledge generally available to one of ordinary skill in the art, to modify the reference or combine reference teachings. Second, there must be a reasonable expectation of success. Finally, **the prior art reference (or references when combined) must teach or suggest all the claim limitations.** The teaching or suggestion to make the claimed combination and the reasonable expectation of success must both be found in the prior art, and not based on applicant's disclosure. *In re Vaeck*, 947 F.2d 488, 20 USPQ2d 1438 (Fed. Cir. 1991). (Emphasis added).

The 35 U.S.C. § 103(a) obviousness rejection of claim 19 is improper because the elements for a *prima facie* case of obviousness are not met. Specifically, the rejection fails to meet the criterion that the prior art references must teach or suggest all the claim limitations.

Regarding claim 19, Dea, So, Abramatic, and Hardiman, either individually, or in any proper combination, do not teach, suggest, or motive Applicants' invention as claimed, namely, Dea, So, Abramatic and Hardiman do not appear to disclose an apparatus for assisting in compressing video data in a computer system including a central processing unit, comprising: "a **video input port** configured to electrically couple to a video unit for receiving video data for a current video frame from streaming video data; a video input buffer coupled to the video input port . . .; a previous frame buffer . . .; an exclusive-OR unit coupled to the video input buffer and the previous frame buffer . . .; and a result buffer coupled to the exclusive-OR unit . . .; a **memory port** coupled to the previous frame buffer and the result buffer, the memory port **independent from the video input port**; and a system memory coupled to the memory port . . ." as claimed by Applicants. Specifically, Applicants' apparatus for assisting in compressing video includes at least a separate video input port for coupling with the streaming video data from a video unit and a memory port for coupling with the system memory.

Therefore, since Dea, So, Abramatic or Hardiman, either individually or in any proper combination, do not teach, suggest, or motivate Applicants' invention as claimed in amended claim 19. Applicants respectfully request that the rejection to claim 19 be withdrawn.

Applicant request entry of this amendment for the following reasons:

(i) The amendment is timely filed;

(ii) The amendment clearly places the application in condition for allowance; and

(iii) The amendment does not require any further search or consideration.

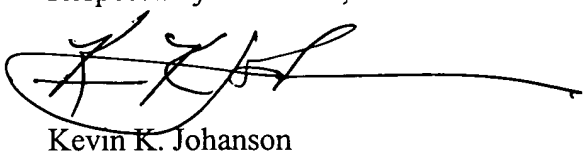
CONCLUSION

After carefully considering the cited prior art, the rejections, and the Examiner's comments, Applicant has amended the claimed invention to clearly distinguish over the cited prior art.

Applicant submits that claims 1 through 7, 9 through 16 and 18 through 20 are clearly allowable over the cited prior art.

Applicant requests the allowance of claims 1 through 7, 9 through 16 and 18 through 20 and the case passed for issue.

Respectfully submitted,



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